Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE 10/602322 **Application Number** STATEMENT BY APPEICANT (Use as many sheets as lecensely) June 24, 2003 **Filing Date First Named Inventor** Farrar, Paul **Group Art Unit** 1763 Unknown **Examiner Name** Attorney Docket No: 1303.096US1 Sheet 1 of 1

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate	
ソソ	US2001/0014524	08/16/2001	Farrar, Paul A.	438	613	02/19/1999	
4	US2002/0034581	03/21/2002	Farrar, Paul A., et al.	427	58	02/20/2001	
7	US-3,959,047	05/25/1976	Alberts, G. S., et al.	156	8	09/30/1974	
	US-5,457,345	10/10/1995	Cook, H. C., et al.	257	766	01/14/1994	
	US-5,461,257	10/24/1995	Hundt, M. J.	257	707	03/31/1994	
	US-5,642,261	06/24/1997	Bond, R. H., et al.	361	704	06/30/1994	
	US-5,693,572	12/02/1997	Bond, R. H., et al.	437	209	01/18/1996	
<u> </u>	US-6,136,689	10/24/2000	Farrar, Paul A.	438	626	08/14/1998	
(11)	US-6,435,396	08/20/2002	Eldridge, Jerome M.	228	33	04/10/2000	

FOREIGN PATENT DOCUMENTS										
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T²				

OTHER DOCUMENTS NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item No (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T		
$\mathcal{N}$		ANONYMOUS, "Combination Process for Final Metal Lines and Metal			
		Terminals*, Kenneth Mason Publications Ltd, Research Disclosure No. 342,			
		England,(Oct. 1992),1 page			
	•	ANONYMOUS, "Process for High Density of Chip Terminals on Large Wafers",			
		Kenneth Mason Publications Ltd, Research Disclosure No. 02, England, (Feb.			
		1993),1 page			
		BABIARZ, A J., "Key Process Controls for Underfiling Flip Chips", Solid State			
		Technology, 40(4), (April 1997),77-8, 81, 83			
		JONES, P, et al., "Bumped Wafers, Worth Their Weight in Gold?", Advanced			
		Packaging, 8(1), (January 1997),54-57			
		MARCOTTE, V. C., "Review of Flip Chip Bonding", Proceedings of the 2nd ASM			
		International Electronic Materials and Processing Congress, 24-28 April 1989,			
		Philadelphia, PA, (1989),73-81			
		MINGES, MERRILL, "Electronic Materials Handbook", Materials Park, OH:			
<u> </u>		ASM International, (1989),301, 440	١		
		PUTTLITZ, KARL J., et al., "Solder Transfer Technique for Flip-Chip and			
$  $ $ $		Electronic Assembly Applications", IEEE Transactions on Components.			
		Packaging and Manufacturing Technology, Part C, Volume 21, No. 3, (July			
$\bot \Psi $		1998),182-188			
		RYAN, J. G., "Technology Challenges for Advanced Interconnects", Advances			
1 4)		in Metallization and Interconnect Systems for ULSI Applications, September 30 -			
L 4V		October 2, 1997, San Diego CA, (1997),1-5			

EXAMINER DATE CONSIDERED 8/28/06

Substitute Disclosure Statement Form (PTO-1449)

- EXAMINER: tritial If reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered, include copy of this form with next communication to applicant. Applicant's unique obtain designation number (optional) 2 Applicant is to place a check mark nere If English language Translation is attached